REMARKS

Claims 1-27 are currently pending in the subject application and are presently under consideration. It is also noted that the subject matter of the reference Le *et al.*, cited herein, and the claimed invention were, at the time the invention was made, subject to an obligation of assignment to Advanced Micro Devices, Inc. Accordingly, a rejection under 35 U.S.C. §103(a) in view of Le *et al.* would not be proper pursuant to the provisions of 35 U.S.C. §103(c).

Favorable reconsideration of the subject patent application is respectfully requested in view of the comments herein.

I. Rejection of Claims 1-15 and 17-26 Under 35 U.S.C. §102(e)

Claims 1-15 and 17-26 stand rejected under 35 U.S.C. §102(e) as being anticipated by Le *et al.* (U.S. 6,690,602 B1). It is respectfully requested that this rejection be withdrawn for at least the following reason. Le *et al.* does not teach or suggest each and every limitation recited in the subject claims.

> A single prior art reference anticipates a patent claim only if it expressly or inherently describes each and every limitation set forth in the patent claim. *Trintec Industries, Inc. v. Top-U.S.A. Corp.*, 295 F.3d 1292, 63 USPQ2d 1597 (Fed. Cir. 2002); *See Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the ... claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The claimed invention relates to a core-based multi-bit memory having a dual-bit dynamic referencing architecture fabricated on the memory core. The referencing architecture provides for *two arrays*, one array fixed at a certain voltage level and a second array fixed at another voltage level. Specifically, independent claim 1, as amended, recites ***a first bit value of a first reference cell of the first reference array averaged with a second bit value of a second reference cell of the second reference array to arrive at the reference voltage.*** Independent claims 13, 17, and 24 recite similar limitation(s). Le *et al.* does not disclose the novel aspect employing a ***second reference array to arrive at the reference voltage.***

Rather, Le *et al.* discloses a plurality of dual bit flash memory cells arranged in a plurality of sectors with each sector having an *associated reference array*. (*See* Abstract)). Specifically, Le *et al.* discloses that dynamic reference A and dynamic reference B make up *the reference array*. Further, Figure 3 of Le *et al.* is directed towards taking an average of bit values associated with the *single reference array*, wherein such average is employed in connection with determining a correct voltage value of a core cell. (*See* Col 5, Lines 44-46). Thus, the cited reference does not teach a ***second reference array*** when averaging bit values. (See Col. 5, Lines 37-40). To that end, Le *et al.* is silent as to ***a first bit value of a first reference cell of the first reference array averaged with a second bit value of a second reference cell of the second reference array to arrive at the reference voltage.***

In view of at least the forgoing, it is respectfully submitted that Le *et al.* does not teach or suggest applicants' invention as recited in the subject claims, and withdrawal of this rejection is requested.

II. Rejection of Claims 13, 16, 24 and 27 Under 35 U.S.C. §102(e)

Claims 13, 16, 24 and 27 stand rejected under 35 U.S.C. §102(e) as being anticipated by Kurihara, *et al.* (U.S. 6,791,880 B1). It is respectfully requested that this rejection be withdrawn for at least the following reason. Kurihara, *et al.* does not teach or suggest each and every limitation recited in the subject claims.

In particular, Kurihara, *et al.* does not disclose ***a first bit value of a first reference cell of the first reference array averaged with a second bit value of a second reference cell of the second reference array to arrive at the reference voltage.*** Instead, the cited reference is directed towards two reference blocks included in a *single core memory array*. (See Col. 5, Lines 54-57). Thus, Kurihara, *et al.* is silent as to a ***first and second reference array.***

In view of at least the forgoing, it is respectfully submitted that Kurihara *et al.* does not teach or suggest applicants' invention as recited in the subject claims, and withdrawal of this rejection is requested.

CONCLUSION

The present application is believed to be in condition for allowance in view of the above comments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 [AMDP975US].

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicants' undersigned representative at the telephone number below.

Respectfully submitted,

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